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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/773,462	02/09/2004	Ju-hyun Lee	1793.1200	3608

21171 7590 09/12/2007

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EXAMINER	
NGO, HUYEN LE	
ART UNIT	**PAPER NUMBER**
2871	

MAIL DATE	DELIVERY MODE
09/12/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/773,462	LEE, JU-HYUN	
	Examiner	Art Unit	
	Julie-Huyen L. Ngo	2871	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 July 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-32* is/are pending in the application.

4a) Of the above claim(s) *3,4,6-16,18 and 20-32* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1, 2, 5, 17 and 19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *7/20/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

Applicant's election with traverse of Species A in Group I (claims 1, 2, 5, 17 and 19) in Paper filed on July 30,2007 is acknowledged.

Applicant's arguments regarding the restriction requirement have been considered; however, the traversal was on the grounds that there is no serious burden on the Examiner in examining all of claims 1-24 inn Group I together. This is not found persuasive since the different locations of the driving circuits, the buffer circuits and the switching circuits recited in claims 3-4, and 6-16, 18 lead to different effects. Also the Examiner has clearly stated the reasons for restriction between inventions of groups I, II and II; and the mutually exclusive characteristics recited in claims 1-24 of different species, which have different structural layouts of the same elements, thus they are not obvious variants based on the current record. The species are independent or distinct from each other and restriction is proper (see page 2-9).

However, Applicant fails to submit evidence or identify such evidence now of record showing the species to be obvious variants or clearly admit on the record that this is the case.

Therefore, the requirement is deemed proper and is considered to be final.

Accordingly, claims 3-4, 6-16, 18 and 20-32 are withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected inventions and species, there being no allowable generic or linking claim. Therefore, ONLY claims 1, 2, 5, 17 and 19 are pending as read on the elected Species.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-2, 5, 17 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Murade (US2001/0030722) in view of Makiko et al. (JP2000-122616) and Aoki et al. (US6177916B1).

Murade discloses (at least in Figs. 2-6) a liquid crystal display (LCD) panel comprising:

Claim 1:

- a liquid crystal panel in which liquid crystal is 108 filled between upper 31 and lower 300 substrates and the liquid crystal is in communication with a display electrode (pixel electrode 14) and a common electrode (counter electrode 32) which face each other;
- a first driving circuit (shift register circuit 221) connected to the liquid crystal panel by a plurality of data lines and which applies a data signal to the liquid crystal panel;

- a second driving circuit (shift register circuit 231) connected to the liquid crystal panel by a plurality of gate lines and which applies a scan signal to sequentially apply the data signal to the liquid crystal panel;
- an electrode pad unit which applies an alignment signal voltage to the liquid crystal panel for alignment of the liquid crystal filled in the liquid crystal panel;
- a first switching circuit (data sampling circuit 101) which performs a switching operation to apply the alignment signal voltage applied via the electrode pad unit to the liquid crystal panel via the data lines

wherein

Claim 2:

- the first switching circuit 101 is placed between the first driving circuit 221 and the liquid crystal panel

Claim 5:

- the first buffer circuit 222 is placed between the first driving circuit and the first switching circuit 101.

Claim 19:

- a liquid crystal panel comprising a plurality of pixels in liquid crystal to display images;
- a driving circuit supplying signals to the plurality of pixels to control the display images;
- an electrode unit to supply an alignment signal voltage to the liquid crystal panel; a switching circuit selectively switching the alignment signal voltage from the

electrode unit to the liquid crystal display panel to align liquid crystal in the liquid crystal panel; and

- a buffer circuit connected to the driving circuit to prevent the alignment signal voltage from flowing to the driving circuit.

However, Murade fails to disclose a liquid crystal display (LCD) panel comprising

- a second switching circuit which performs a switching operation to apply the alignment signal voltage applied via the electrode pad unit to the liquid crystal panel via the gate lines; where the second switching circuit is placed between the liquid crystal panel and the electrode pad unit (claim 17)
- first and second buffer circuits, which prevent the alignment signal voltage from being applied to the first and second driving circuits.

Makiko et al. teach (Fig. 1 and abstract) forming a liquid crystal display (LCD) panel comprising a second switching circuit 125, which performs a switching operation to apply the alignment signal voltage applied via the electrode pad unit to the liquid crystal panel via the gate lines; where the second switching circuit is placed between the liquid crystal panel and the driving circuit 123; however, Murade discloses that the driving circuit is placed between the electrode pad and the liquid crystal panel, thus the second switching circuit is placed between the liquid crystal panel and the electrode pad unit.

Aoki et al. teach (at least Fig. 1, col. 3, lines 51- col. 4, line 10) forming a liquid crystal display (LCD) panel comprising first and second buffer circuits 12, which prevent the alignment signal voltage from being applied to the first and second driving circuits.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to further modify a liquid crystal display device as Murade disclosed with:

(a) a second switching circuit that performs a switching operation to apply the alignment signal voltage applied via the electrode pad unit to the liquid crystal panel via the gate lines; where the second switching circuit is placed between the liquid crystal panel and the electrode pad unit for switching liquid crystal impressing voltage, as taught by Makiko (abstract);

(b) first and second buffer circuits, which prevent the alignment signal voltage from being applied to the first and second driving circuits first and second buffer circuits, which prevent the alignment signal voltage from being applied to the first and second driving circuits for reducing parasistic capacitance loads thus improving the bandwidth characteristics of the bus lines even where the number of the bus lines increase, as taught by Aoki et al.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure:

Komiya et al. (US006940214B1) an insulator substrate (110) provided with a display pixel region (200) comprising an electroluminescence element (160) having a

cathode (167), emissive layer (166), and anode (161), and with first and second TFTs for driving the element. Surrounding the display pixel region (200), a peripheral drive circuit region (251) having a third TFT for driving each pixel is further provided on the insulator substrate (110).

Kubota et al. (US006492972B1) disclose a data signal line driving circuit which sequentially forms a plurality of sampling signals and continuously samples input signals to output such input signals, in response to the plurality of sampling signals, wherein the sampling signals respectively represent sampling periods thereof which are different from each other, and a pulse width of each of the sampling signals is prescribed to be small so that rising and falling of each of the sampling signals do not overlap each other.

Zhang et al. (US 6806862 B1) disclose a liquid crystal display device 540 including the line-sequential driver IC chip 512, common signal lines D1-D384, CMOS-type TFT analog switches 514, block control lines BL1-BL10, the gate driver circuit 516, the display part 518, a shift register circuit 542, and a buffer circuit 544. The shift register circuit 542 and the buffer circuit 544 form a circuit, which generates the block signal BL. The shift register circuit 542 is supplied with a start pulse SP and clock signals CL and/CL.

Contact Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Julie-Huyen L. Ngo whose telephone number is (571) 272-2295. The examiner can normally be reached on M-Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Nelms can be reached on (571) 272-1787. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Julie-Huyen L. Ngo
Primary Examiner
Art Unit 2871